In the Claims:

1. (Currently Amended) A method of forming isolating regions of a semiconductor device, the method comprising:

providing a workpiece, the workpiece having at least one first region and at least one second region, ~~the at least one first region comprising at least one first active area, the second region comprising areas for at least one second active area,~~ the workpiece having a top surface;

forming at least one first active area in said at least one first region;

patterning the first region with at least one first trench after said step of forming said first active area, the first trench having sidewalls, a bottom, and a first width and a first depth within the workpiece;

forming a first insulating layer over the at least one first trench sidewalls and bottom;

depositing a semiconductive material in the at least one first trench over the first insulating layer~~, wherein the semiconductive material is recessed beneath the workpiece top surface~~;

depositing a photo resist for patterning shallow second trenches over said first and second regions of said substrate;

patterning ~~the~~ both said first and second regions, each region patterned with ~~region with~~ at least one second trench, the second trench having a second depth within the workpiece, ~~wherein the second depth~~ that is less than the first depth and a second width greater than said first width, said second trenches in said first region being located over said first trenches so as to recess said first insulating layer adding semiconductor material in said first trenches;

depositing an insulating material in the at least one second trench and in the semiconductive material recess of the at least one first trench; and then

forming at least one second active area in the second region.

2. (Original) The method according to Claim 1, wherein the at least one first active area comprises at least one high voltage device, and wherein the at least one second active area comprises at least one low voltage device.

3. (Canceled)

4. (Original) The method according to Claim 1, wherein depositing a semiconductive material comprises depositing doped polysilicon or undoped polysilicon, wherein forming the insulating layer over the at least one first trench sidewalls and bottom comprises:

forming a thin nitride layer over the at least one first trench sidewalls and bottom; and

forming a thin oxide layer over the thin nitride layer.

5. (Original) The method according to Claim 1, further comprising, before depositing an insulating material in the at least one second trench and in the semiconductive material recess of the at least one first trench, depositing a second insulating layer over the at least one second trench and over the semiconductive material recess of the at least one first trench.

6. (Original) The method according to Claim 5, wherein depositing the second insulating layer comprises:

forming a thin silicon dioxide layer over the at least one second trench and over the semiconductive material recess of the at least one first trench; and

forming a thin silicon nitride layer over the thin silicon dioxide layer.

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Currently Amended) A method of forming isolating regions of a semiconductor device, the method comprising:

providing a workpiece, the workpiece having at least one first region and at least one second region, ~~the at least one first region comprising at least one high voltage active area, the second region comprising areas for at least one low voltage active area,~~ the workpiece having a top surface;

forming at least one high voltage active area in said at least one first region;

patterning the first region with at least one deep trench after forming said at least one high voltage active area, the deep trench having a first width, sidewalls, a bottom, and a first depth within the workpiece;

forming a first insulating layer over the at least one deep trench sidewalls and bottom;

depositing a semiconductive material in the at least one deep trench over the first insulating layer~~, wherein the semiconductive material is recessed beneath the workpiece top surface~~;

recessing said semiconductive material beneath the workpiece top surface;

forming a hard mask having portions over said at least one first region and over said at least one second region;

~~masking the at least one first region;~~

patterning the portion of said hard mask over said at least one second region ~~with~~and transferring said hard mask pattern to form at least one shallow trench in said second region and leaving the portion of said hard mask over said first region in place such that said first region is not further patterned, the shallow trench having a second depth and a second width within the workpiece, wherein the second depth is less than the first depth and the second width is greater than said first width;

removing ~~the~~ any remaining hard mask from over ~~the~~ at least one first region and said at least one second region;

depositing an insulating material in the at least one shallow trench and in the semiconductive material recess of the at least one deep trench; and

forming at least one low voltage active region in the second region.

11. (Original) The method according to Claim 10, wherein depositing an insulating material in the semiconductive material recess of the at least one deep trench comprises forming shallow trench isolation over the deep trenches.

12. (Original) The method according to Claim 10, wherein depositing the semiconductive material comprises depositing doped polysilicon or undoped polysilicon, wherein forming the insulating layer over the at least one deep trench sidewalls and bottom comprises:

forming a thin nitride layer over the at least one deep trench sidewalls and bottom; and

forming a thin oxide layer over the thin nitride layer.

13. (Original) The method according to Claim 10, further comprising, before depositing an insulating material in the at least one shallow trench and in the semiconductive material recess of the at least one deep trench, depositing a second insulating layer over the at least one shallow trench and over the semiconductive material recess of the at least one deep trench.

14. (Original) The method according to Claim 13, wherein depositing the second insulating layer comprises:

forming a thin oxide layer over the at least one shallow trench and over the semiconductive material recess of the at least one deep trench; and

forming a thin nitride layer over the thin silicon dioxide layer.

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Original) The method according to Claim 10, wherein patterning the first region with at least one deep trench comprises:

depositing a hard mask over the workpiece top surface;

patterning the hard mask with the deep trench pattern;

patterning the workpiece using the hard mask as a mask; and

removing the hard mask.

19. (Original) The method according to Claim 18, wherein depositing the hard mask comprises depositing Boron-doped Silicon Glass (BSG).

20. (Currently Amended) The method according to Claim 10, wherein said steps of forming a hard mask ~~masking the at least one first region~~ and patterning the hard mask over said at least one second region with at least one shallow trench ~~comprise~~ comprising the steps of:

~~depositing a hard mask over the workpiece and the patterned deep trench in the first region;~~

depositing a photoresist over the hard mask;

patterning the photoresist with the at least one shallow trench pattern;

patterning the hard mask with the photoresist pattern;

removing the photoresist;

patterning the workpiece using the hard mask as a mask; and

removing the hard mask.

21. (Previously Presented) The method according to Claim 20, wherein depositing the hard mask comprises depositing high density plasma (HDP) silicon dioxide.

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (New) The method according to claim 10 wherein said at least one low voltage active region in the second region is formed after said insulating material is deposited in the at least one shallow trench and the at least one deep trench.

26. (New) The method according to claim 10 wherein said at least one low voltage region in the second region is formed prior to said step of patterning the first region with at least one deep trench.